ABSTRACT OF THE DISCLOSURE

A data processing apparatus (1) can implement the execution of a virtual machine instruction based on an execution routine specified by the native instruction of a CPU (2) and has an address converting unit (3) capable of sequentially converting an address output from the CPU into the address of the native instruction by utilizing the address of a prepared execution routine in response to the application of a prescribed condition. The address converting unit reads a virtual machine instruction to be executed next and prepares the address of an execution routine corresponding thereto in parallel with the execution of the execution routine by the CPU based on the address of the native instruction which is sequentially converted. Accordingly, it is possible to reduce the overhead of a processing of loading the virtual machine instruction and a processing of executing an instruction in accordance with the execution routine which is caused by an address calculation processing based on the load processing. Consequently, it is possible to increase the speed of a data processing to be carried out by a virtual machine program described in a virtual machine instruction.